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(54) **Linear feedback shift register.**

(57) A linear feedback shift register for inclusion in a VLSI circuit. During a test function for the VLSI circuit, the shift register can be programmed into an LSSD test mode, or to generate test patterns for the VLSI circuit, and to perform a corresponding signature analysis on hashing functions on the VLSI response to the test pattern. The linear feedback shift register can be programmed on the VLSI chip to perform any of these test functions. During normal VLSI circuit operation, the shift register is transparent to logic signals carried by the VLSI circuit.

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LINEAR FEEDBACK SHIFT REGISTER

Background of the Invention

The present invention relates to VLSI circuit testing techniques. Specifically, a linear feedback shift register for inclusion on a VLSI integrated circuit is described which is programmable for carrying out several common test functions.

The complexity of very large scale integrated circuits, VLSI, renders the testing of such circuits very difficult and expensive. To alleviate the difficulty, circuit testability has been designed into the VLSI circuit. In the past, as outlined in a paper reported in the IEEE Journal of Solid State Circuits, Vol. SC-15, No. 3 June 1980, entitled "Built-In Test for Complex Digital Integrated Circuits", a built-in register provides for an input signal drive for circuits under test, and a test answer evaluator in the form of another register permits evaluation of the result of applying the input signal drive to the circuit under test.

The built-in registers have been used as a scan generator to apply a test pattern to the device and compare the circuit response to the test patterns with the applied test patterns. The register may be operated in a serial shift register linear (LSR) mode, permitting the desired test pattern to be serially entered into the register and then latched to provide a desired parallel input to a circuit under test. The circuit under test is then rendered operable and the response to the input is parallel loaded in another LSR mode register. The response to the test is then serially read out to determine whether the circuit under test functioned appropriately. These techniques are generically referred to as level sensitive scan design, LSSD.

More sophisticated testing is performed through the use of random pattern generation and corresponding signature analysis operating the LSR as a linear feedback shift register. The random pattern is generated by a linear differential shift register with appropriate feedback to generate a polynomial pseudo-random number. The polynomial is applied to the circuit under test. The response of the circuit under test to the continuously changing random number is "hashed" or compressed by another linear differential shift register operated as a signature analyzer to preserve any detected errors. At the end of the pattern generation sequence, the hashed result is serially read from the signature analyzer to determine whether the circuit under test performed appropriately.

The on-chip testing techniques using SRL registers all produce hardware overhead for the chip. Additionally, the linear feedback shift register requires feedback connections and control lines adding to the device pin out.

Summary of the Invention

It is an object of the invention to provide a linear feedback shift register useful for onboard testing of VLSI circuits.

It is a more specific object of this invention to provide a linear feedback shift register which is programmable to provide random pattern generators, signature analyzers and to perform as an LSSD latch.

These and other objects of the invention are provided by a linear feedback shift register which is preferably implemented in NMOS or CMOS. The feedback shift register can be operated in a normal bypass mode whereby the device is

transparent to VLSI circuit signals during normal operation. Alternatively, in a test function for a VLSI circuit, the register can be used in an LSSD mode whereby individual bits can be shifted serially into or out of the register cells. Additional programming of the register will permit its use as a test pattern generator or signature analyzer.

This invention, defined more particularly by the claims which follow, comprises a multicell register which can be programmed to carry out the above testing functions. Each cell includes a one bit register connected to receive either normal data from the VLSI circuit, or the output signal from one or more serially connected exclusive NOR circuits. The exclusive NOR circuits are connected to provide a logical function of the logic level from a previous or later cell such that test pattern generation, signature analysis or LSSD functions may be provided.

The individual cells in a preferred embodiment are programmable on the VLSI chip. When programmed in the pattern generator mode, the exclusive NOR gates and one bit register provide for each cell the function:

$$\text{FEEDBACK} \ \overline{\oplus} \ \text{SHIFT},$$

wherein FEEDBACK comprises a common feedback signal from the last cell for generating a desired polynomial, and SHIFT comprises the output of a previous cell. In a signature analyzer mode, the individual cells of the register may be programmably connected to provide the logical function:

$$\text{FEEDBACK} \ \overline{\oplus} \ \text{SHIFT} \ \overline{\oplus} \ \text{INPUT}$$

where INPUT is an applied logic level from the circuit under test.

Description of the Figures

Figure 1 is a block diagram of a VLSI circuit which includes onboard linear differential feedback shift registers as testing circuits.

Figure 2 is a functional block diagram showing a plurality of cells which comprise the linear feedback shift register of Figure 1.

Figure 3 illustrates the connections of each cell of the linear differential shift register to derive an LSSD register.

Figure 4 illustrates the connections of each cell of the linear differential shift register to perform a pattern scan polynomial.

Figure 5 illustrates the connections of each cell of the linear differential shift register to perform a signature analysis.

Figure 6 is a schematic illustration of each cell of the linear differential shift register of Figure 2.

Figure 7 is a typical one bit register L used in the cell of Figure 6.

Description of a Preferred Embodiment

Referring to Figure 1, there is shown a VLSI integrated circuit which includes onboard test capability utilizing a linear feedback shift register according to a preferred embodiment. The VLSI circuit is preferably in NMOS and includes circuits 12 and 15, as well as two linear feedback shift registers, hereinafter LFSR 13 and LFSR 14. Each of the LFSRs includes a plurality of stages, S_0

through S_n, that register shown in the normal operation wherein input data along the plurality of inputs I_n-I_0 of the VLSI circuit are transferred through cells S_0 through S_n to the circuit 12 under test. Similarly, the LFSR 14 receives outputs from circuit 12 and transfers them in a normal operation directly to circuit 15.

With the VLSI circuit of Figure 1, it is possible to program each LFSR 13 and LFSR 14 through external pin connections on the VLSI circuit to perform any one of four basic test functions, including the level sensitive scan design (LSSD), as well as the use of test generation polynomials and corresponding hashing of the result. With this latter test technique, as described in the literature previously referenced, the LFSR 13 can be programmed to generate a test pattern which is analyzed in the LFSR 14. Although hardwired external pin connections are utilized in the present example, other techniques such as preprogramming the VLSI mask to effect at least some of the connections is possible. Utilizing the circuit of the preferred embodiment, the LFSR 13 and 14 can be implemented in NMOS technology using only twelve (12) additional devices than is currently employed with a standard LSSD latch. Thus, with a minimum of hardware overhead it is possible to achieve the additional capability of test pattern generation and the hashing of the result.

Referring now to Figure 2, an LFSR of a preferred embodiment is shown including cells S_0-S_4. Cell S_4 is typical of all cells of the LFSR and for simplicity, the control lines and input-output lines have been shown for a single cell S_4 in Figure 2. Normal INPUT/OUTPUT lines are shown for the cell, as well as the following INPUT/OUTPUT connections:

FBI SHIFT IN SHIFT OUT

Additionally, the following control lines to each cell are provided:

Test 1	Test 2	IN
$\overline{FD}$	FD	$\overline{IN}$

Throughout the discussion, it is understood that when FD or IN are at one logic level, the complements $\overline{FD}$ and $\overline{IN}$ are at an opposite logic level. Referring to Figure 3, the use of the LFSR is shown in Figure 3 having connections between the SHIFT OUT line of each cell, and a SHIFT IN line of each cell. Additional to the wiring of each cell as shown in Figure 3, certain clock signals and control signals are applied as follows.

In the LSSD operation, data is fed into the SHIFT IN input of the S_0 cell and under the clock sequence of Test 1 and Test 2 which are non-overlapping, inverse clock signals. The data appearing on the SHIFT IN input of cell S_0 is propagated under control of the Test 1, Test 2 clock pulses. In normal LSSD operation, sufficient serial data bits are serially shifted into the linear feedback shift register until cells S_0 through S_4 obtain parallel data for applying to a circuit under test.

Similarly, the LFSR 14 of Figure 1 is clocked to read out parallel loaded data appearing from the normal input lines from circuit 12. LFSR 14 is serially read out such that the SHIFT OUT pulse of the last cell S_4 provides for the serial data which was presented in parallel format to the inputs of register cells S_0 through S_4.

Referring now to Figure 4, a pattern scan generator is shown implementing the LFSR of Figure 2. The programmed connections between cells S_0 and S_4 are shown, wherein, as in the LSSD operation, the SHIFT OUT connection of each cell is connected to the SHIFT IN connection of each

subsequent cell. Additionally, there is a feedback signal provided to individual selected cells to generate the polynomial of a particular scan pattern. Shown in Figure 4 are the connections to generate a polynomial having the form $X^5 + X^4 + X^2 + 1$. The output lines of the LFSR will generate on a pseudo-random basis a test pattern for applying to the circuit 12 of VLSI circuit 11.

The remaining connections of the LFSR of Figure 4 are such that the IN connection is 0 and the FD connection is maintained at a logic 1 level. The Test 1 and Test 2 signals are clock signals which are complementary inverse and non-overlapping clock signals.

Referring now to Figure 5, the hashing function for signature analysis of a circuit under a pattern scan of Figure 4 is shown. In the circuit of Figure 5, each of the cells S_0 through S_4 are programmed through hardwiring pin terminals provided on the VLSI circuit 11 such that, as previously the SHIFT OUT connection of each cell is applied to a SHIFT IN connection of the subsequent cell. In carrying out the hashing function, however, the first cell S_0 has a SHIFT IN connection isolated from the S_4 SHIFT OUT connection. Additionally, the FBI connection of each cell is connected to receive a feedback signal from the SHIFT OUT connection of S_4.

In carrying out the hashing function, once again clock pulses are applied to the Test 1 and Test 2 connections having an inverse relationship to each other and which are non-overlapping. Additionally, the IN and FD control lines are maintained at logic 1 levels for the hashing function. Input lines of the cells S_0 through S_4 are connected to receive the output from the circuit 12 under test. The hashing result is clocked from the LFSR by returning to the configuration of Figure 3, wherein the

contents of the entire register may be serially clocked out of the register.

In normal non-test operation of the VLSI circuit, Test 1, Test 2, IN and FD are maintained at zero logic levels, thus rendering the circuit transparent to the normal VLSI circuit operation.

Thus, it is seen with an LFSR having the general configuration of Figure 2, any one of four modes of operation may be effected, including a normal operation wherein the LFSR is transparent to data on the VLSI circuit, an LSSD function, a pattern generation function, and a hashing function.

Referring now to Figure 6, there is shown one cell S_4 of the LFSR of the preferred embodiment. It is to be understood that the remaining cells of the LFSR are identical to that of Figure 6.

The central portion of each cell comprises a register 23, the register being a one bit register which can accept input from a normal data path for the VLSI circuit, or a test path through gate 27. Gate 27 is an FET which, when appropriately clocked by a Test 1 signal, will provide for a test signal to be applied to the one bit register 23. At the output of the one bit register 23 is a gate 28 which is clocked in accordance with a test 2 signal. As was explained with respect to the inter-connection of the cells of Figures 3 through 5, Test 1 and Test 2 are inverse clock signals which do not overlap. The signal propagated through gate 28 under control of Test 2 clock signal, is inverted by inverter 30. A further gate 32 is used to propagate the results to the SHIFT OUT connection of each cell.

In order to carry out the LSSD shift function, wherein data is serially loaded into one LFSR and serially read out of a second LFSR as described with respect to Figure 3, the input test pattern is applied serially to the SHIFT IN connection. As the clock pulses are applied to the Test 1 and Test 2 input, the bit pattern will be loaded in all of the cells at the conclusion of the appropriate number of clock pulse cycles.

Two exclusive NOR circuits, 19 and 20, are shown which permit the carrying out of the pattern generation function and the hashing function. The exclusive NOR gates 19 and 20 comprise two cross-coupled FETs, each having a load transistor 19a and 20a connected as load circuits to a voltage source V_{tt}. One input of the first exclusive NOR circuit 20 is connected to receive the output of the second exclusive NOR circuit 19 as well as an input signal common to the input of latch 23. A control gate 22 permits connection of the input signal to one input of exclusive NOR gate 20 under control of the IN and $\overline{IN}$ control lines.

The second exclusive NOR gate, also comprising two cross-coupled FETs with a load impedance comprising a transitor 19a, receives as one input a SHIFT IN signal, and as the other input a FEEDBACK INPUT (FBI) signal. The FBI signal is inverted through inverter 24, and controlled by a gate 26. Gate 26 includes a series FET transistor and parallel FET transistor under control of signals FD and $\overline{FD}$.

In the pattern generation mode the IN control signal is held to be 0 and the FD signal is held to be 1. Thus, the LFSR will produce a suitable random number having a polynomial defined by the connections of Figure 4.

During the hashing mode, the IN port is held at 1 and data from the circuit under test enters through the input of gate 22. The FD control signal is held at logic 1, permitting the feedback signal to be propagated to the input of exclusive NOR circuit 19.

The one bit register 23 is shown more particularly in Figure 7. It has been found in practice that the register described in pages 3384 & 3385 of IBM Technical Disclosure Bulletin, Vol. 25, No. 7A, December 1982, which shows a cross-coupled register having a transistor in one of the feedback paths between cross-coupled transistor pairs, performs well in the LFSR. Figure 7 demonstrates the use of the one bit register described in the aforesaid Technical Disclosure Bulletin. The device comprises first and second transistor series pairs 41, 42 cross-coupled to form a latch. One of the cross-coupling lines includes a transitor 43, which as noted in the aforesaid Technical Disclosure Bulletin, improves the speed of the latch device.

Transistors 45 and 46, driven from the nodes of the latch, provide an output which is normally fed to the output gate transistor 28.

Additionally, an input gate 47 is included which, under the control of NORM IN control line, permits the normal input to the register 23 to be received in lieu of a test input through gate 27.

The foregoing description of the individual cells of the LFSR of a preferred embodiment are implemented in NMOS technology, as is the remaining circuitry of the VLSI circuit. Typical voltage connections for the device include the standard 5.0 ± .25 volt power supply voltages denominated as V_{++} or VDD. It is also possible to set

V_{++} equal to zero during normal operation to avoid unnecessary power consumption.

Thus there has been described a linear feedback shift register, LFSR, capable of performing multiple test functions on a VLSI circuit. These functions are carried out by connections between cells of the LFSR, and by the application of certain clock signals. The LFSR provides for an improved test capability over standard LSSD techniques, with only minimal addition of hardware and pin out requirements for the VLSI circuit. Those skilled in the art will recognize yet other embodiments of the invention to be described more particularly by the claims which follow.

CLAIMS

1. A programmable linear feedback shift register for self-testing a VLSI circuit, said register having a plurality of one bit stages, each stage comprising:

a second exclusive NOR circuit (19) for receiving a binary shift signal from a preceediing stage, and a feedback signal (FBI);

a first exclusive NOR circuit (20) for receiving a first logical signal from said second exclusive NOR circuit, and an input signal;

a cross-coupled register (23) connected to receive a signal from said VLSI circuit during normal VLSI circuit operation, and a signal from said first exclusive NOR circuit during a test operation;

an inverter circuit (30) for receiving an output signal from said cross-coupled register, said inverter circuit supplying a shift signal for application to a subsequent stage's second exclusive NOR circuit; and

means (27) for coupling said first exclusive NOR circuit output during a first test interval to said cross-coupled register, and means (28) for coupling an output signal from said cross-coupled register to said inverter during a second test interval.

2. A programmable linear feedback shift register as claimed in claim 1 wherein said second exclusive NOR circuit (19) comprises:

a pair of cross-coupled FETs having one input connected to receive a shift signal, and a remaining input; and a feedback gate (26) for applying a binary feedback signal to said remaining input and applying a logical zero binary state signal to said remaining input in the absence of a feedback pulse.

3. A programmable linear feedback shift register as claimed in claim 2 wherein said first exclusive NOR circuit (20) is coupled through a gate circuit means (22) to receive an input signal is response to an enabling INPUT signal.

4. A VLSI circuit including a register for performing testing functions for a remaining portion of said VLSI circuit comprising:

a multicell register, each of said cells comprising:

a one bit register (23);

a first exclusive NOR gate (20);

a second exclusive NOR gate (19);

said first exclusive NOR gate having a first input connected to receive the output signal from said second exclusive NOR gate, and a second input adapted to receive a logical INPUT signal;

said second exclusive NOR gate having first and second inputs adapted to receive a SHIFT IN signal and FEEDBACK signal; and

means for connecting the output of said first exclusive NOR gate to said one bit register input and the output of said

one bit register to an input of the second exclusive NOR gate of another of said cells, during respective first and second test intervals.

5. A VLSI circuit as claimed in claim 4 further comprising a gate circuit (22) connected to control a said logical INPUT signal entering said first exclusive NOR gate second input.

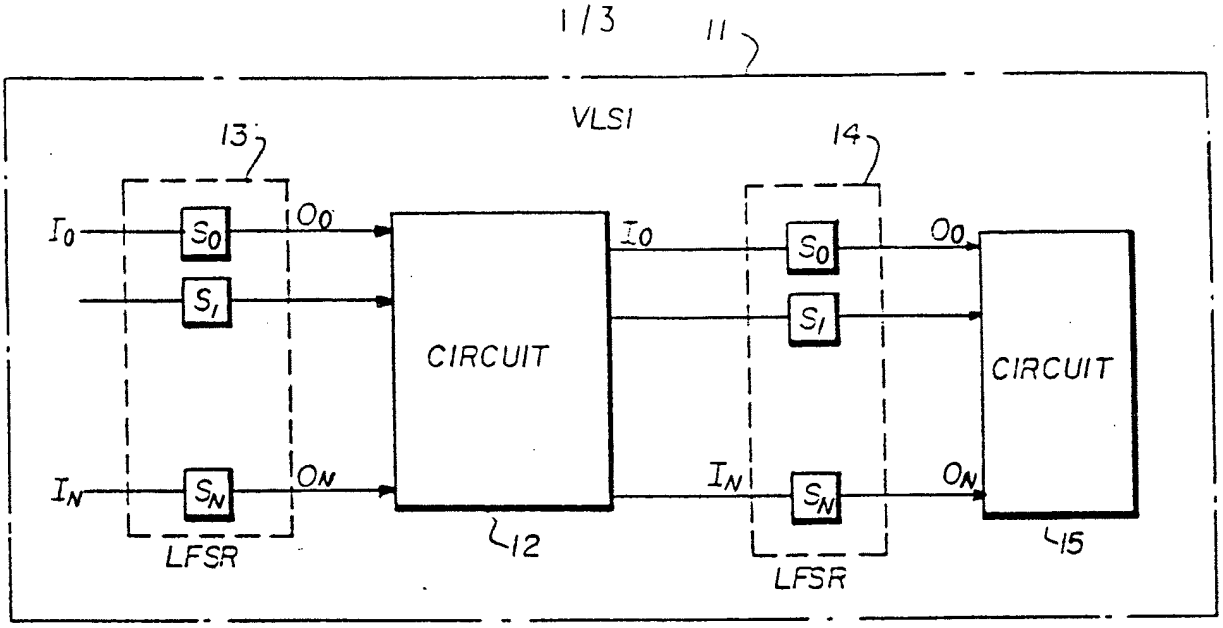

FIG 1

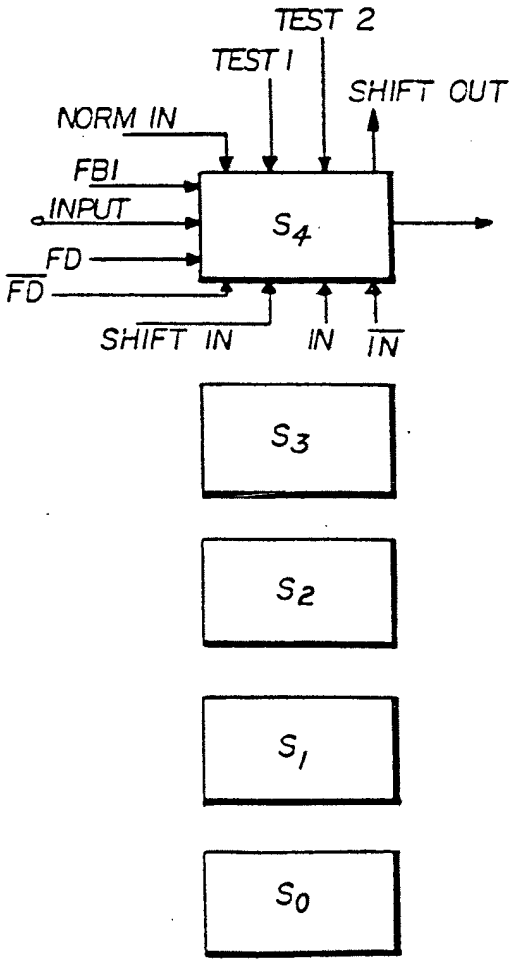

FIG 2

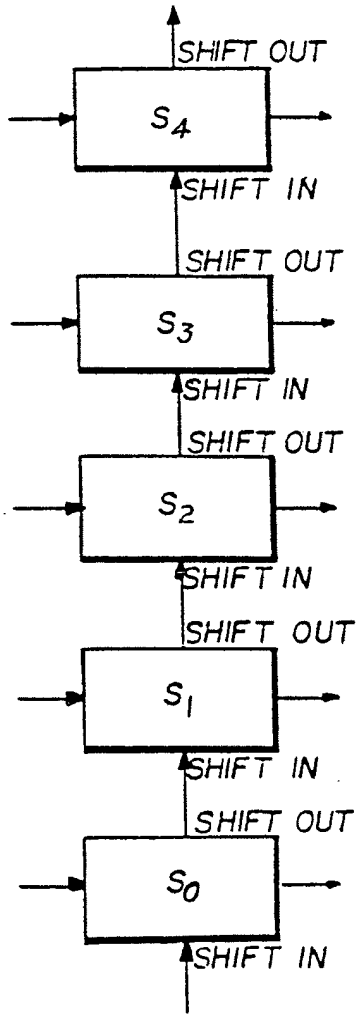

FIG 3

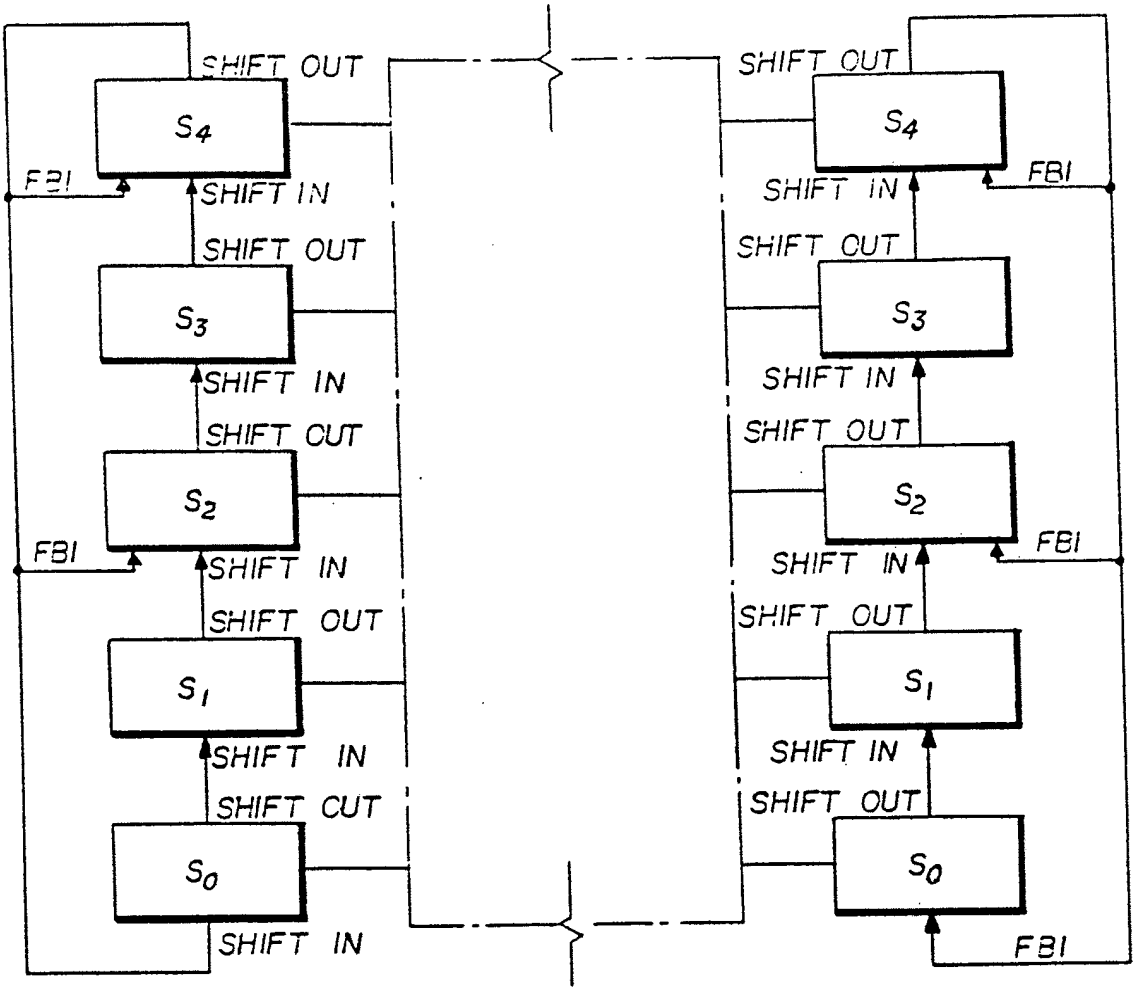

FIG 4

FIG 5

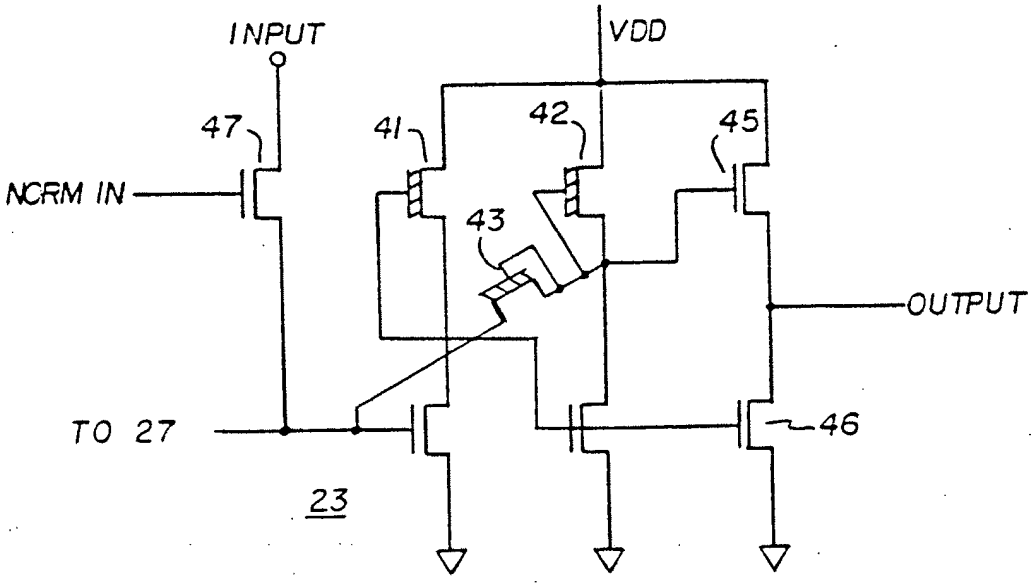

FIG 7

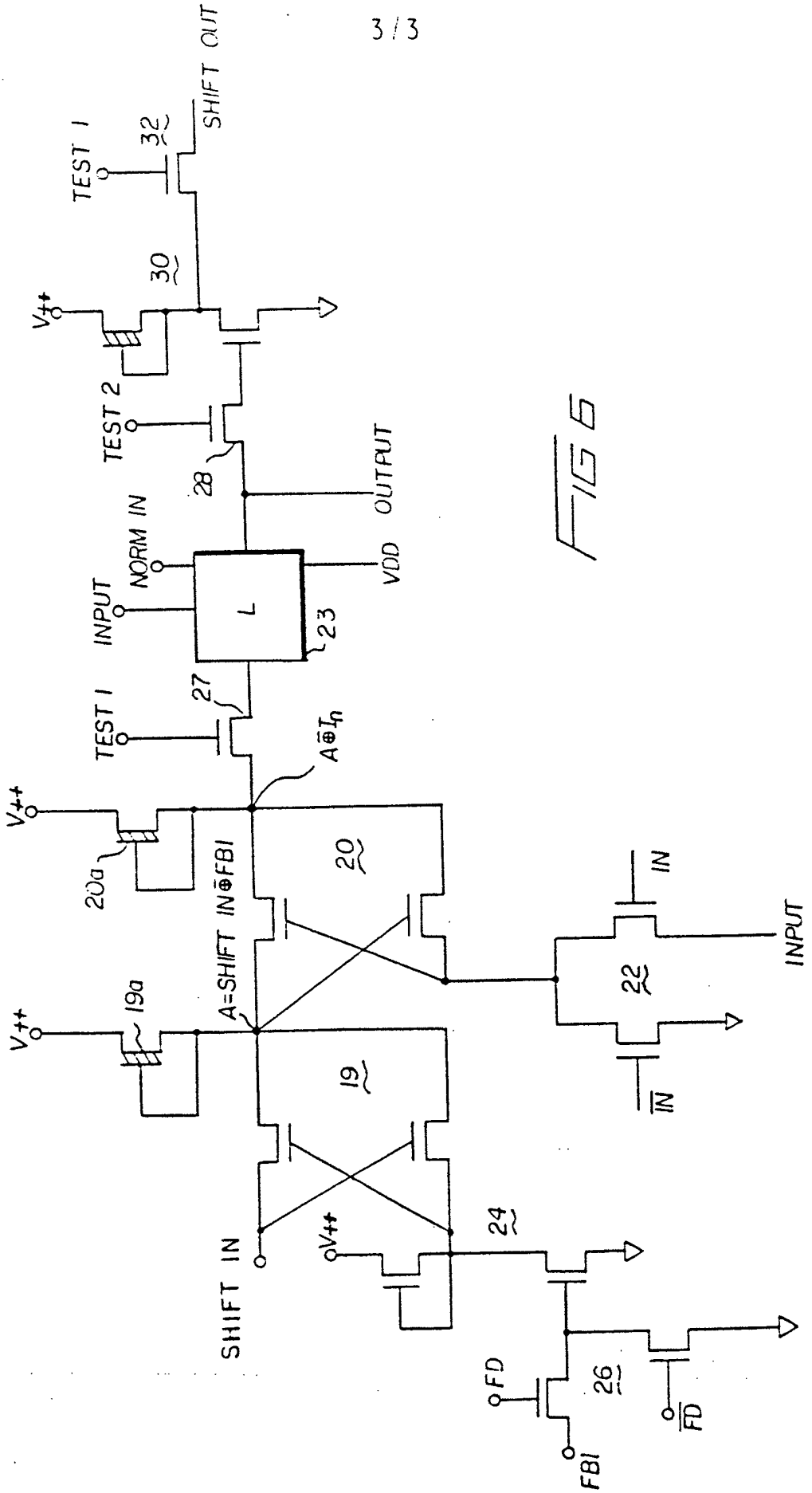
SHIFT OUT
TEST 1
32
30
V++
TEST 2
28
OUTPUT
NORM IN
INPUT
L
VDD
23
TEST 1
27
A⊕Īn
V++
20a
20
IN⊕FBI
IN
INPUT
V++
19a
A=SHIFT
22
IN
19
SHIFT IN
V++
24
FD
26
FD
FBI

FIG 6

European Patent Office

EUROPEAN SEARCH REPORT

0148403
Application Number

EP 84 11 4661

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	ELECTRONICS, vol. 56, no. 5, 10th March 1983, pages 109-124, New York, US; R.W. COMERFORD et al.: "Special report: A little extra circuitry on chip and special software lets VLSI test itself chip by chip and board by board" * Pages 110-115 *	1,4,5	G 01 R 31/28 G 11 C 19/00 G 06 F 11/26 H 03 M 9/00 G 06 F 7/58
A	EP-A-0 046 499 (IBM) * Figures 1,2; pages 6-8 *	1,4	
D,A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 25, no. 7A, December 1982, pages 3384-3385, New York, US; H.H. CHAO et al.: "High speed general purpose register with resistive feedback and bootstrapped input control gates"		

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

G 01 R 31/28
G 06 F 7/58

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	25-02-1988	CRECHET P.G.M.

CATEGORY OF CITED DOCUMENTS

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